

FIG. 1

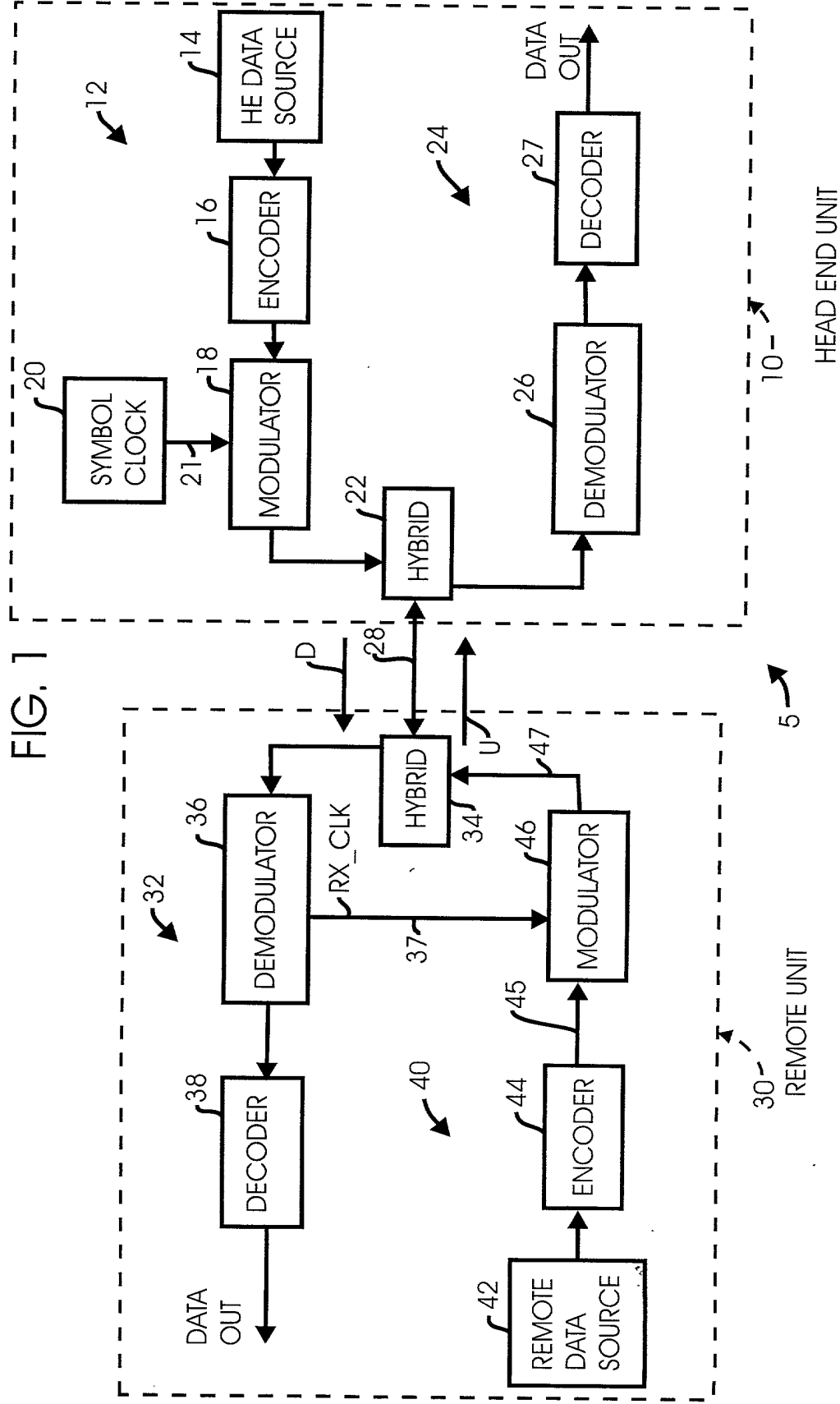


FIG. 2

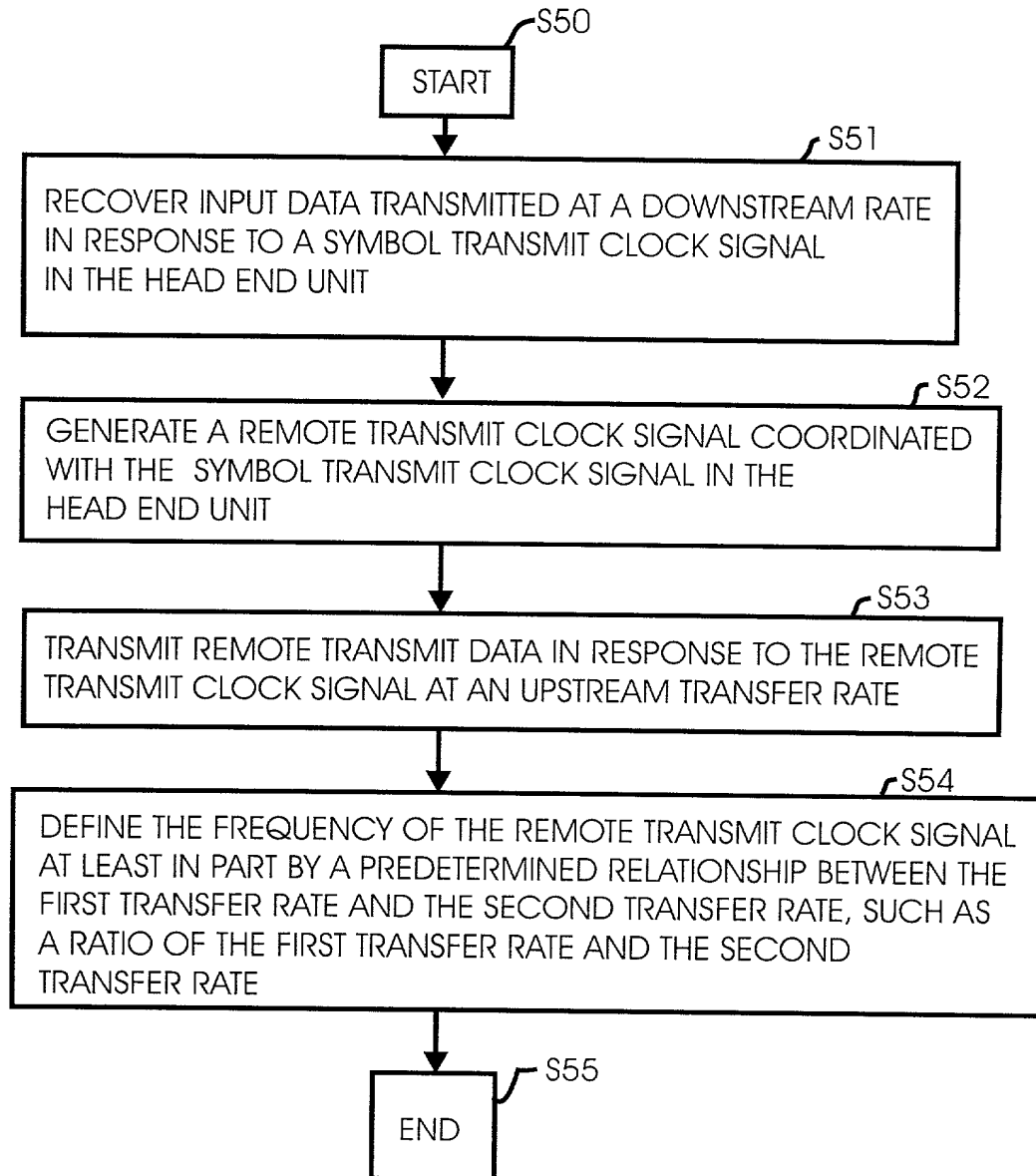


FIG. 3

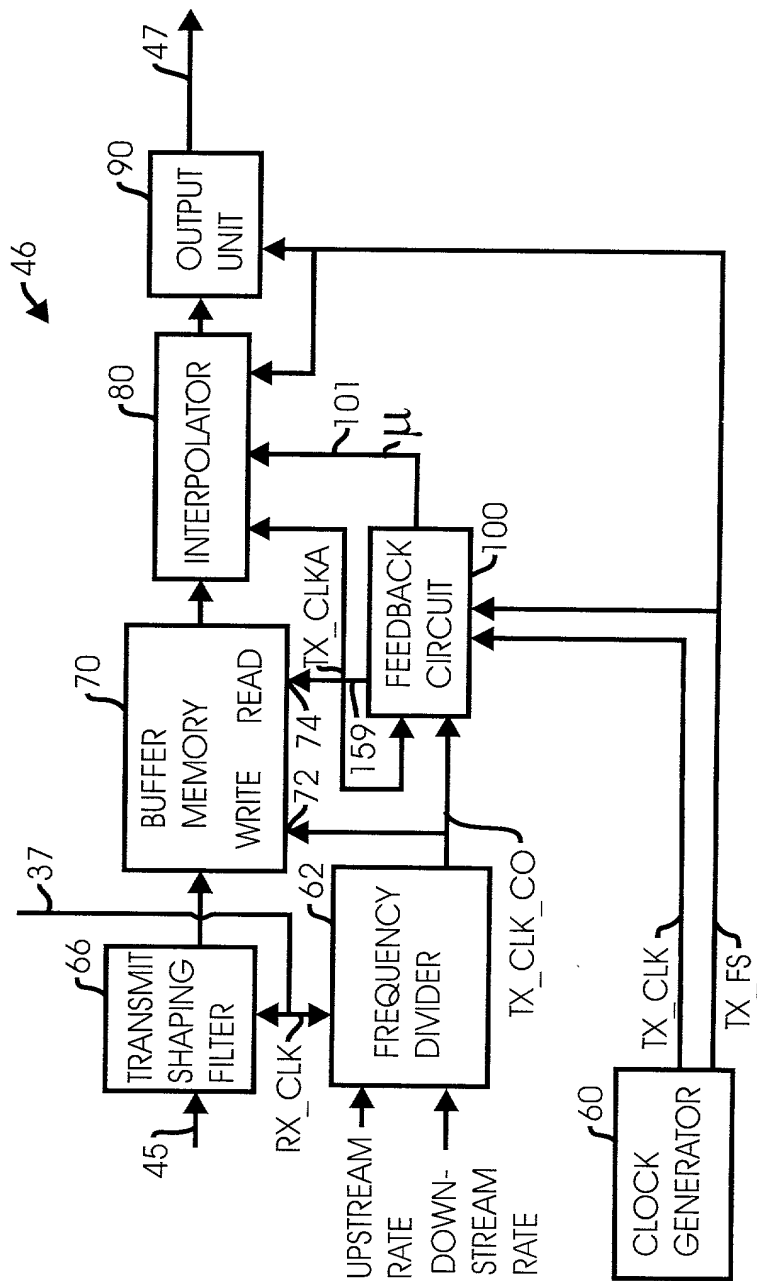


FIG. 4

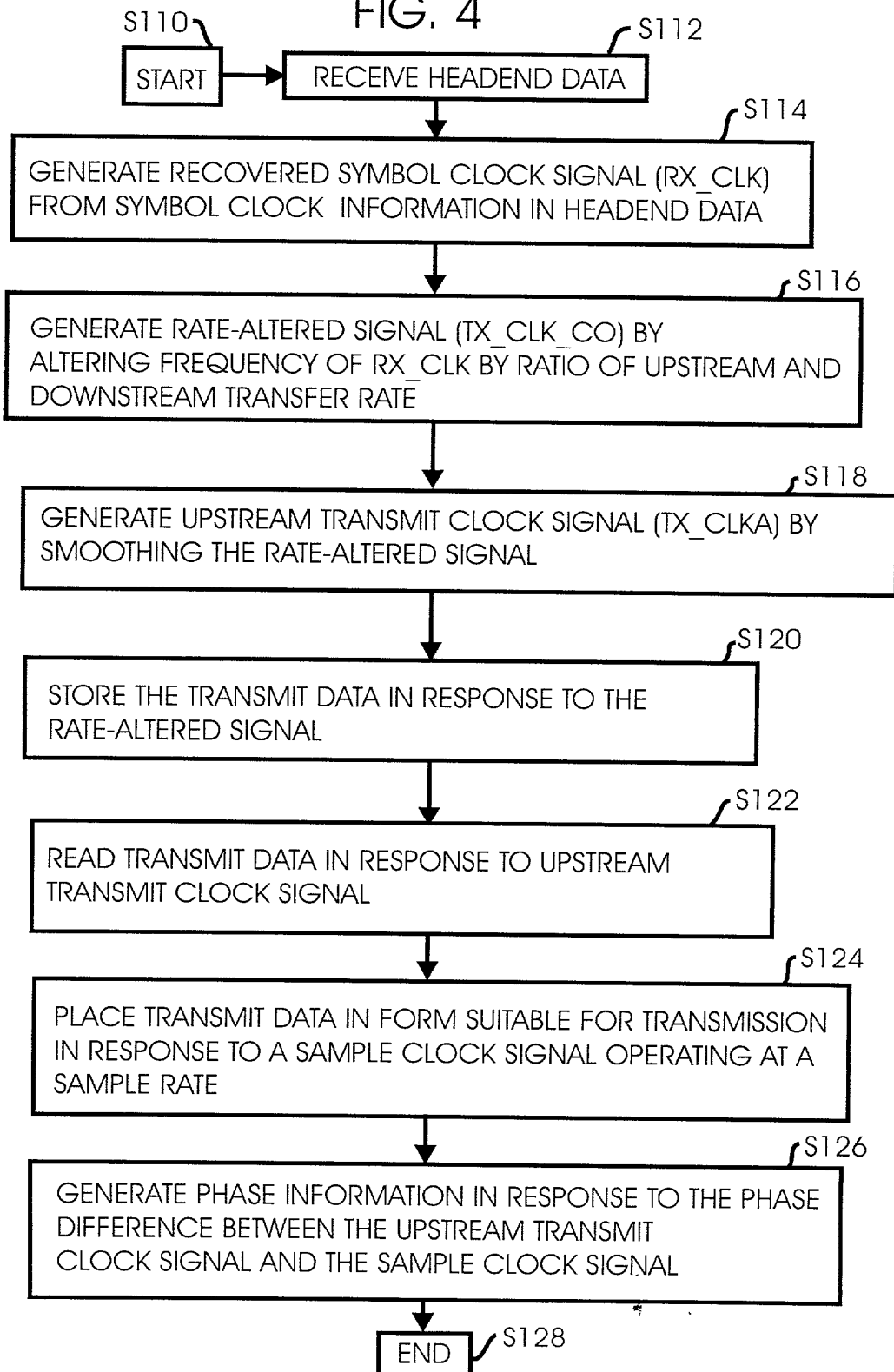
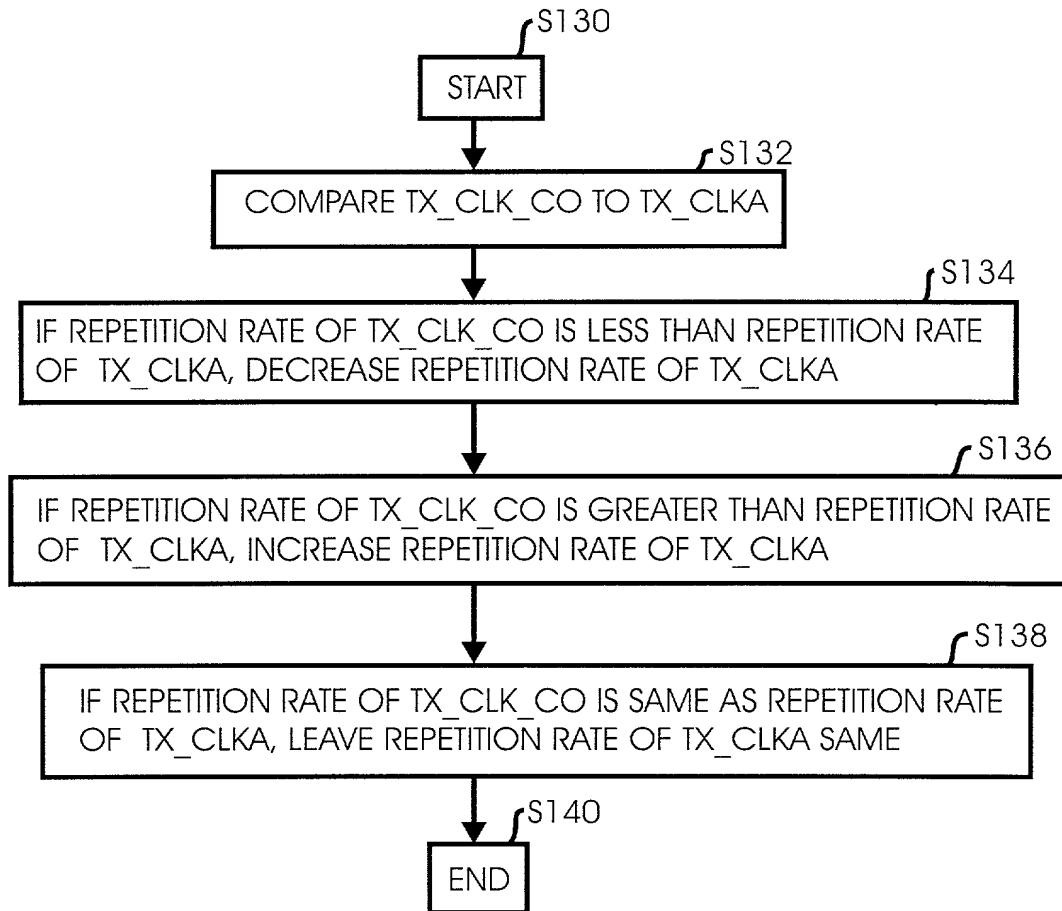


FIG. 5

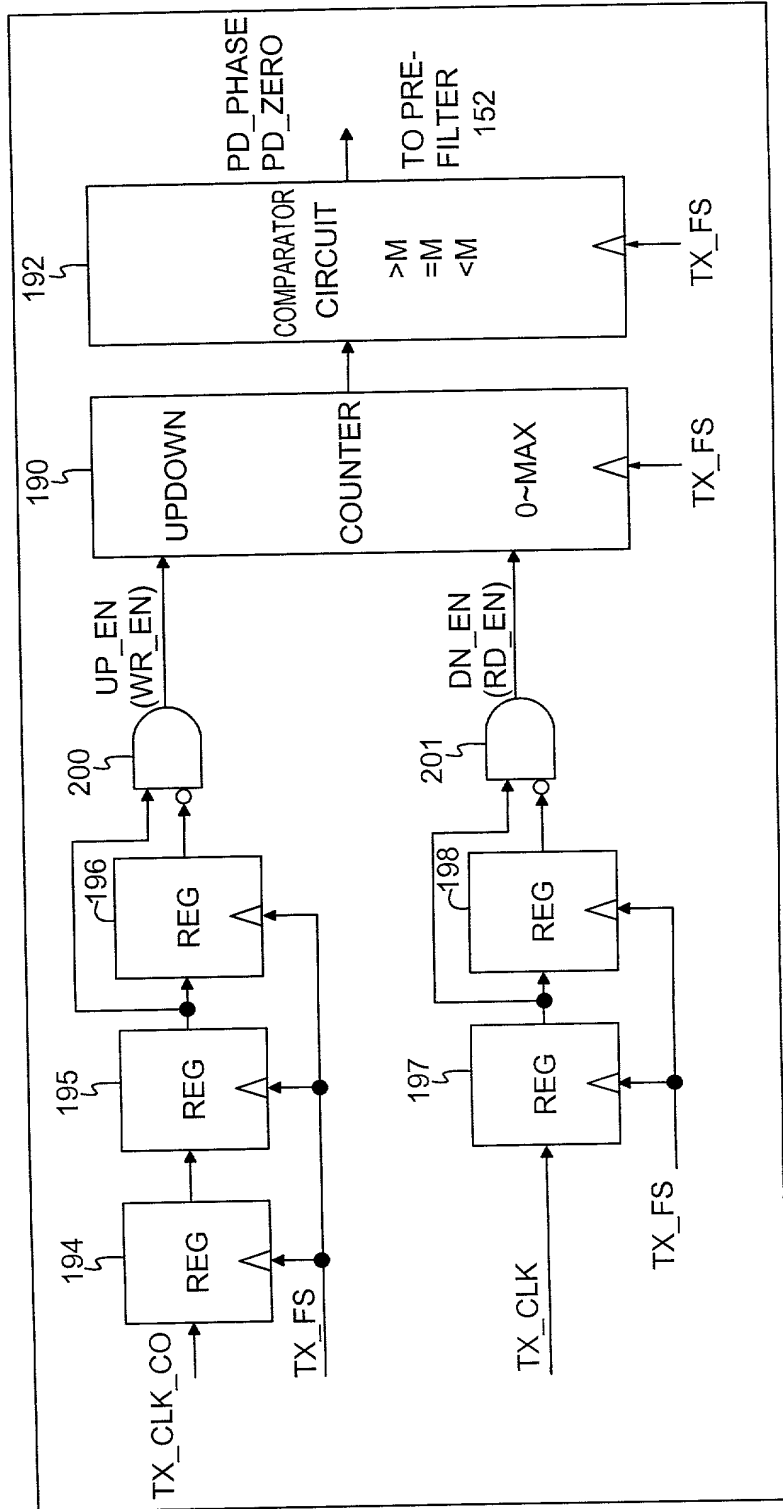


[illegible]

FIG. 1 is a block diagram of a digital PLL circuit. The circuit includes a feedback loop with two adders (174 and 176) and a register (170). The output of the feedback loop is fed into a divider (178) which has two outputs, 1 and 0. The output of the divider is fed into a counter (180) and an AND gate (182). The counter (180) is also fed by RX_CLK and has a RESET input connected to the output of the AND gate (182). The output of the counter (180) is fed into a register (172) which is also fed by RX_CLK. The output of the register (172) is fed into the AND gate (182). The output of the AND gate (182) is TX_CLK_CO. The output of the divider (178) is also fed into the AND gate (182). The output of the AND gate (182) is also fed into the register (170) which is also fed by RX_CLK. The output of the register (170) is SUM_RATE_NEXT.

7/9

FIG. 8

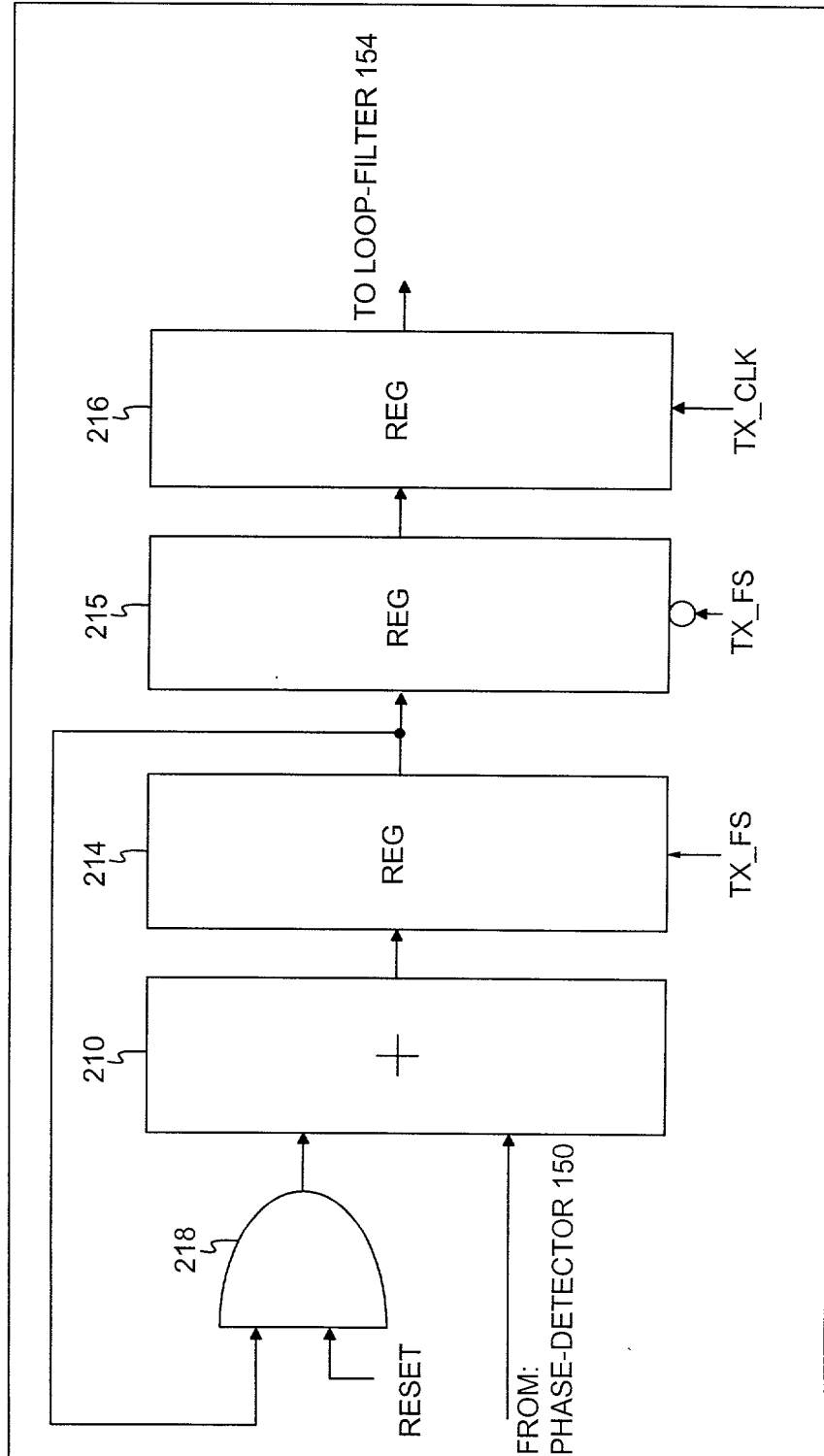


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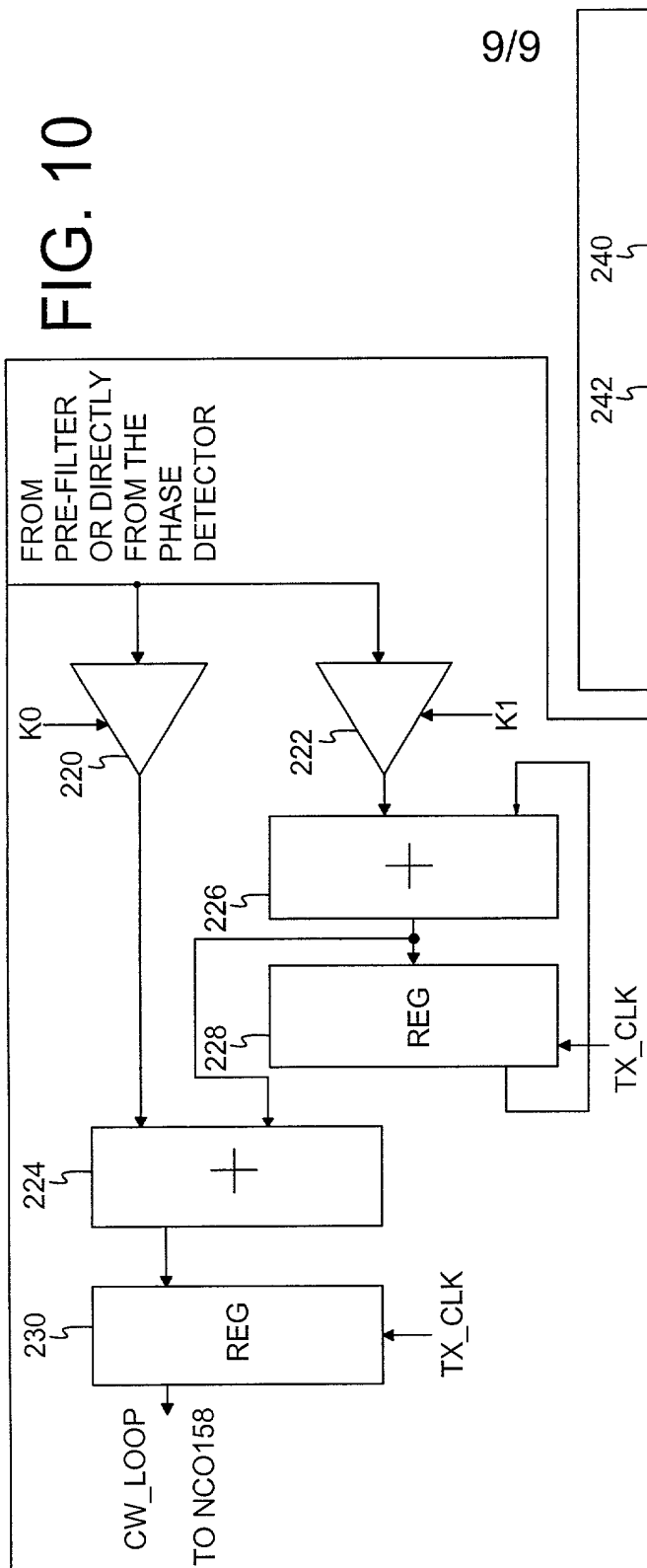
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8/9

FIG. 9



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9/9

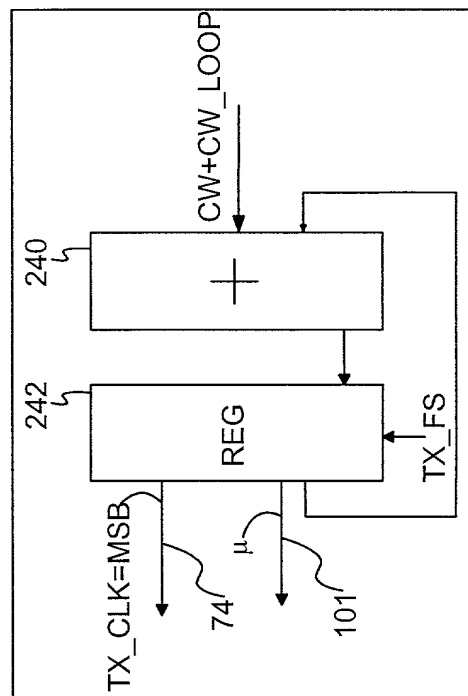


FIG. 11